This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A method of handling bus operations in a computer system having a processor for forming a plurality of bus operation information structures, a plurality of memory spaces for containing the bus operation information structures and a sequencer for processing the bus operation information structures to perform the bus operations, comprising the steps of:

sequentially forming each bus operation information structure by the processor in the memory spaces, said each bus operation information structure including both a command and data ~~to be transferred~~;

upon forming each bus operation information structure, setting control over the bus operation information structure to the sequencer;

determining whether the sequencer has control over a first one of the bus operation information structures;

upon determining that the sequencer has control over the first bus operation information structure, processing the first bus operation information structure by the sequencer;

determining whether the sequencer has control over a second one of the bus operation information structures; and

upon determining that the sequencer has control over the second bus operation information structure, processing the second bus operation information structure by the sequencer,

wherein the computer system includes a central processing unit (CPU) and a bus adapter, the bus adapter including the processor, the sequencer and the memory spaces, the CPU being communicatively coupled to the bus adapter.

2. (original): A method as defined in claim 1, wherein the computer system further has a queue of pointers and each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure is ready for processing, comprising the further steps of:

upon forming the first bus operation information structure, placing a pointer identifying the first bus operation information structure in the queue of pointers by the processor; and

reading the pointer identifying the first bus operation information structure from the queue of pointers by the sequencer before processing the first bus operation information structure.

3. (original): A method as defined in claim 2 comprising the further step of:

setting control over each bus operation information structure to the sequencer by placing the pointer identifying each bus operation information structure in the queue of pointers.

4. (original): A method as defined in claim 2, wherein the queue of pointers supplies a start flag to the sequencer whenever the queue of pointers contains a pointer that has not been read by the sequencer, comprising the further steps of:

asserting the start flag after placing the pointer identifying the first bus operation information structure in the queue of pointers;

determining that the sequencer has control over the first bus operation information structure by receiving the start flag by the sequencer and reading the pointer identifying the first bus operation information structure from the queue of pointers.

5. (original): A method as defined in claim 2, wherein the queue of pointers is a first queue of pointers and the computer system further has a second queue of pointers of which each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed, comprising the further steps of:

after processing the first bus operation information structure, placing a pointer identifying the first bus operation information structure in the second queue of pointers by the sequencer;

reading the pointer identifying the first bus operation information structure from the second queue of pointers by the processor; and

forming a third bus operation information structure in the same memory space

containing the first bus operation structure.

6. (original): A method as defined in claim 1, wherein the computer system further has a queue of pointers and each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed, comprising the further steps of:

after processing the first bus operation information structure, placing a pointer identifying the first bus operation information structure in the queue of pointers by the sequencer;

reading the pointer identifying the first bus operation information structure from the queue of pointers by the processor; and

forming a third bus operation information structure in the same memory space containing the first bus operation structure.

7. (original): A method as defined in claim 6 comprising the further step of:

setting control over each bus operation information structure to the processor by placing the pointer identifying each bus operation information structure in the queue of pointers.

8. (original): A method as defined in claim 6, wherein the queue of pointers supplies a complete flag to the processor whenever the queue of pointers contains a pointer that has not been read by the processor, comprising the further steps of:

asserting the complete flag after placing the pointer identifying the first bus operation information structure in the queue of pointers;

determining that the processor has control over the first bus operation information structure by receiving the complete flag by the processor and reading the pointer identifying the first bus operation information structure from the queue of pointers.

9. (original): A method as defined in claim 1 comprising the further step of:

upon forming the first bus operation information structure, sending a signal from the processor to the sequencer to start processing the first bus operation information structure.

10. (original): A method as defined in claim 9 comprising the further steps of:

upon forming each bus operation information structure by the processor, associating the bus operation information structure with a link to a next bus operation information structure; and

after processing each bus operation information structure by the sequencer, determining which bus operation information structure is to be processed next by reading the associated link to the next bus operation information structure.

11. (original): A method as defined in claim 10, wherein each bus operation information structure includes a link field which indicates the next bus operation information structure, comprising the further step of:

upon forming each bus operation information structure by the processor, setting the link field of the bus operation information structure to the next bus operation information structure to associate the bus operation information structure with the link.

12. (original): A method as defined in claim 9, wherein each bus operation information structure includes an owner field which indicates whether the processor or the sequencer has control over the bus operation information structure, comprising the further steps of:

upon forming each bus operation information structure, setting the owner field to the sequencer by the processor to set control over the bus operation information structure to the sequencer; and

after processing each bus operation information structure, setting the owner field to the processor by the sequencer.

13. (original): A method as defined in claim 9 comprising the further steps of:

before forming each bus operation information structure, setting control over the bus operation information structure to the processor;

after processing the first bus operation information structure, determining whether the sequencer or the processor has control over the second bus operation information structure; and

upon determining that the processor has control over the second bus operation information structure, waiting for the processor to send a signal to the sequencer to start processing the second bus operation information structure.

14. (currently amended): A method as defined in claim 9, ~~wherein the computer system includes a central processing unit (CPU) and a bus adapter, the bus adapter includes the processor, the sequencer and the memory spaces,~~ comprising the further steps of:

sending a plurality of input/output (I/O) messages from the CPU to the bus adapter;

receiving the I/O messages at the processor in the bus adapter; and

forming the bus operation information structures from the I/O messages.

15. (currently amended): A computer system comprising:

a bus across which information is transferred;

a plurality of memory spaces containing bus operation information structures describing bus operations to be performed on the bus, each of said bus operation information structures including both a command and data ~~to be transferred~~;

a plurality of control indicators indicating control status over the bus operation information structures;

a sequencer connected to the memory spaces, to the control indicators and to the bus to perform the bus operations on the bus upon processing the bus operation information structures, the sequencer performing the bus operation described by said each of said bus operation information structures if one of the control indicators indicates that the sequencer has control over the bus operation information structure; and

a processor connected to the memory spaces, to the control indicators and to the sequencer to sequentially form the bus operation information structures in the memory spaces and to generate the control indicators causing the sequencer to process the formed bus operation information structures;

~~and~~ wherein the sequencer processes a first one of the bus operation information structures upon receiving a first one of the control indicators and the sequencer processes a second one of the bus operation information structures upon

completion of processing the first bus operation information structure if a second one of the control indicators indicates that the sequencer has control over the second bus operation information structure; and

wherein the computer system includes a central processing unit (CPU) and a bus adapter, the bus adapter including the processor, the sequencer and the memory spaces, the CPU being communicatively coupled to the bus adapter.

16. (original): A computer system as defined in claim 15 wherein:

the control indicators include a queue of pointers, each pointer being set to identify one of the bus operation information structures when the identified bus operation information structure is ready for processing;

after forming the bus operation information structures, the processor sends the pointers to the queue of pointers identifying the formed bus operation information structures in the order that the bus operation information structures were formed;

the sequencer reads the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers and processes the bus operation information structures in the same order; and

upon completing processing the first bus operation information structure, the sequencer proceeds to process the second bus operation information structure if the queue of pointers contains a pointer for the second bus operation information structure.

17. (original): A computer system as defined in claim 16 wherein:

the queue of pointers supplies a start flag to the sequencer whenever the queue of pointers contains a pointer that has not been read by the sequencer;

the sequencer proceeds to process a next one of the bus operation information structures upon completing processing a previous one of the bus operation information structures if the start flag is supplied to the sequencer and upon receiving the start flag if none of the bus operation information structures is currently being processed.

18. (original): A computer system as defined in claim 15 wherein:

the control indicators include a queue of pointers, each pointer being set to

identify one of the bus operation information structures when the identified bus operation information structure has been processed by the sequencer and the memory space containing the processed bus operation information structure is available for a new bus operation information structure to be formed therein;

after processing the bus operation information structures, the sequencer sends the pointers to the queue of pointers identifying the available memory spaces in the order that the bus operation information structures contained therein were processed;

the processor reads the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers and forms the next bus operation information structure in one of the available memory spaces; and

upon completing forming the first bus operation information structure, the processor proceeds to form the second bus operation information structure if there is at least the one available memory space.

19. (original): A computer system as defined in claim 18 wherein:

the queue of pointers supplies a complete flag to the processor whenever the queue of pointers contains a pointer that has not been read by the processor;

the processor proceeds to form a next one of the bus operation information structures upon completing forming a previous one of the bus operation information structures if there is the at least one available memory space and upon receiving the complete flag if none of the memory spaces is currently available.

20. (original): A computer system as defined in claim 15 wherein:

each bus operation information structure includes the control information indicating control status over the bus operation information structure;

the sequencer performs the bus operation described by each bus operation information structure if the control information within the bus operation information structure indicates that the sequencer has control over the bus operation information structure after processing a previous one of the bus operation information structures or if the sequencer receives a start signal;

the processor forms the control information within the bus operation information structures in the memory spaces and sends the start signal to the sequencer informing the sequencer to start processing the first bus operation

information structure;

the sequencer processes the first bus operation information structure upon receiving the start signal and processes a second one of the bus operation information structures upon completion of the first bus operation information structure if the control information in the second bus operation information structure indicates that the sequencer has control over the second bus operation information structure.

21. (currently amended): A computer system as defined in claim 20 ~~further comprising:~~

~~a bus adapter including the processor, the memory spaces and the sequencer~~, wherein the processor is ~~being~~ operative to form the bus operation information structures from received input/output (I/O) messages; and

~~a central processing unit~~ the CPU is connected to the bus adapter at the processor and operative according to software programming to prepare the I/O messages and to send the I/O messages to the bus adapter, the I/O messages defining I/O operations to be performed through the bus.

22. (original): A computer system as defined in claim 20 wherein:

the processor sets the control information for each bus operation information structure to indicate that the sequencer has control over the bus operation information structure upon forming the bus operation information structure and before sending the start signal to the sequencer; and

the sequencer sets the control information for each bus operation information structure to indicate that the processor has control over the bus operation information structure after processing the bus operation information structure.

23. (original): A computer system as defined in claim 20 wherein:

the sequencer does not process the second bus operation information structure if the control information for the second bus operation information structure indicates that the sequencer does not have control over the second bus operation information structure and the sequencer waits to receive the start signal from the processor before processing the second bus operation information structure.

24. (original): A computer system as defined in claim 20 wherein:

each bus operation information structure includes an owner field containing the control information for the bus operation information structure; and

the owner field of each bus operation information structure is set by the processor after forming the bus operation information structure to indicate that the bus operation information structure has been formed and may be processed by the sequencer.

25. (original): A computer system as defined in claim 20 wherein:

each bus operation information structure includes link information indicating a next one of the bus operation information structures to be processed by the sequencer after processing a current one of the bus operation information structures; and

the sequencer determines which one of the bus operation information structures is the next bus operation information structure from the link information of the current bus operation information structure and determines whether to begin processing the next bus operation information structure from the control information of the next bus operation information structure.

26. (original): A computer system as defined in claim 25 wherein:

each bus operation information structure includes a link field containing the link information; and

the link field of each bus operation information structure is set by the processor to indicate the next bus operation information structure upon forming the current bus operation information structure.